REMARKS

This paper is responsive to a Final Office Action dated November 5, 2003. Claims 9-17 were previously withdrawn in response to the Examiner's assertion that these claims are drawn to a nonelected group. Prior to this amendment, claims 1, 4-8, 18, 21-24, and 26-29 were pending. After canceling claims 1-8, 19-20, and 23-29, amending claims 18 and 22, and adding claims 30 and 31, claims 18, 21-22, and 30-31 remain pending.

In Section 3 of the Office Action claims 1, 4-8, 18, 21-24, and 26-29 have been rejected as unpatentable under 35 U.S.C. 103(a) with respect to Matsunaga (US Patent 5,510,918). Referencing Fig. 4, the Office Action states that Matsunaga depicts an ITO layer (d1), a second conductive layer (d2) of Mo, Ti, Ta, or W overlying the ITO, and a third conductive layer (d3) of Al overlying the second conductive layer. The Office Action also states that it would have been obvious to use such a structure in either an IC or an LCD reflector. This rejection is traversed as follows.

An invention is unpatentable if the differences between it and the prior art would have been obvious at the time of the invention. As stated in MPEP § 2143, there are three requirements to establish a *prima facie* case of obviousness.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when

> combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck* 947 F.2d 488, 20 USPQ2d, 1438 (Fed. Cir. 1991).

In accordance with the above-stated first *prima facie* requirement, the references themselves must suggest a reason to either modify a reference, or the knowledge generally must provide a motivation to modify the reference in such a way as to make the claimed invention obvious. Generally, Matsunaga is concerned with minimizing the gate terminal resistance and, more specifically, minimizing resistance between Al and ITO layers (col. 1, ln. 41-47). Figs. 2-4 describe a pixel consisting of a TFT, an ITO layer, and a latching capacitor (col. 3, ln. 42-54).

The source and drain electrodes are described as consisting of an N+ semiconductor layer (d0), the second conductive layer (d2) overlying d0, and the third conductive layer d3 overlying d2 (col. 7, ln. 16-37). This explanation describes Fig. 3. The only specific description of Fig. 4 occurs at col. 9, ln. 43-67, where the latching capacitor is explained. Specifically, the ITO layer is described as having a step. Matsunaga states that, "(e)ven if the transparent electrode ITO1 is broken at the stepped portion of the electrode PL1 of the latching capacitor Cadd, this defect is compensated by the island region which is constructed of the second conductive film d2 and the third conductive film d3 formed cross that step" (col. 9, ln. 61-67). Thus, the "island" structure (d2/d3) is a fail-safe interconnect.

While Matsunaga describes an interconnect structure, the claimed invention describes an ozone resistant LCD reflector. Neither is there a suggestion that Matsunaga's interconnect be modified to form an

LCD reflector. First, Matsunaga does not discuss the issue of ozone cleaning, or the deleterious effects associated with ozone cleaning. The use of Mo is even suggested as a d2 material. The Mo/Al (d2/d3) combination of materials is the example used in the Background Section of the instant application to illustrate the problems associated with ozone cleaning (see Fig. 1b). The claimed invention resulted from the realization that ozone cleaning damages the conventional Al/Mo structures in response to the differential etch rates, and the simultaneous understandings that the Mo material can be replaced with a substitute material having a higher etch resistance than the overlying electrode layer (Al). Matsunaga does not appear to appreciate the ozone etch rate differential. Likely, because his LCD fabrication process does not include any ozone stripping.

Second, even though Matsunaga is describing LCD circuitry and pixels, he fails to mention a combination of d1/d2/d3 layers as useful in forming a reflector structure. The combination is only cited as being useful as an interconnect. Specifically, claim 22 recites the third layer as being an LCD reflector. Matsunaga does not describe his d3 layer as having such a use. Alternately stated, Matsunaga's d3 layer is likely to be too small (in area) to be an effective reflector, since it is being used for a different purpose.

"Therefore, an examiner may often find every element of a claimed invention in the prior art. If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue....To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the examiner to show a motivation to combine the references that would

create the case of obviousness. In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art reference for combination in the manner claimed." *In re Rouffet*, 47 USPQ2d 1453, 1457-1458 (1998).

Since Matsunaga fails to appreciate the ozone resistance of his interconnect structure, and because he fails to appreciate the structure's usefulness as a reflector, Matsunaga cannot be said to suggest a modification that points to the claimed invention's ozone resistant LCD reflector structure. It is a cornerstone of obviousness analysis that the prior art reference have the same purpose (solve the same problem) as the claimed invention.

Further, the Office Action has not demonstrated that the modification of the cited the prior art reference points to the reasonable expectation of success in the present invention, which is the second requirement of the obviousness analysis. That is, neither the Office Action nor the Matsunaga reference suggests the use of the claimed invention structure as a commercially viable LCD reflector. Neither does the reference suggest that the claimed reflector structure is likely to be practical in commercial fabrication processes using ozone stripping.

The third requirement to support a *prima facie* case of obviousness requires that the combination of references disclose all the elements of the claimed invention. Matsunaga describes his d2 layer elements as Cr, Mo, Ti, Ta, and W. The claimed invention's second layer elements (as amended) include TaN, Cu, Al, and Al compounds. There are no common materials between the two groups. Thus, Matsunaga's d2 layer is a different claim element than the second layer recited in claims

18 and 22. Since Matsunaga neither explicitly describes all the elements of the claimed invention, not suggests a modification that makes the claimed invention obvious, the Examiner is requested to withdraw the rejection.

It is believed that the application is in condition for allowance and reconsideration is earnestly solicited.

Respectfully submitted,

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